OpenComRTOS:

Formally developed RTOS for Heterogeneous Systems

Bernhard H.C. Sputh, Eric Verhulst, and Vitaliy Mezhuyev Email: {bernhard.sputh, eric.verhulst, vitaliy.mezhuyev}@altreonic.com

http://www.altreonic.com

From Deep Space to Deep Sea



Outline



- History of Altreonic
- OpenComRTOS Information
- Performance Figures
- Conclusions

History of Altreonic



3

- Eonic (Eric Verhulst): 1989 2001
 - Developed Virtuoso a Parallel RTOS (sold to Wind River Systems);
 - Communicating Sequential Processes as foundation of the "pragmatic superset of CSP";
- Open License Society: 2004 now
 - R&D on Systems and Software Engineering;
 - Developed OpenComRTOS using Formal Methods

Visit us at Booth 11-102

- Altreonic: 2008 now
 - Commercialises OpenComRTOS;
 - Based in Linden (near Leuven) Belgium;

28/02/2010

OpenComRTOS Factsheet 1

- CSP inspired Real-time Operating System;
- Formally designed and developed;
- Small code size (typically 5 10 KiB);
- Network centric;
- Support for Heterogeneous Systems;
- Currently available Ports:
 - Posix32 and Win32
 - ARM Cortex M3
 - Leon3, Xilinx Microblaze, MLX-16
 - XMOS (experimental, under development)



Services offered by Hubs



- Event Synchronisation on a Boolean value;
- Semaphore Synchronisation with a counter;
- Port Synchronisation and exchanging a packet, i.e. data transport (CSP Channel like);
- Resource Locking mechanism, with ownership;
- FIFO Buffered packet communication;
- Memory Pool For the allocation of memory;



Virtual Single Processor programming Model



- This means: "Transparent access to any entity in the system."
- This is possible due to the separation of Topology and Application.
 - Topology: Defines the Processing Entities (Nodes) and the communication Links between them.
 - Application: Tasks, Hubs and their interactions.







VSP Workflow 2



Define the Application using Tasks, Hubs, and Interactions

VSP Workflow 3 Altreoni - 0 × Semaphore_W_SP.ove - Open Visual Environment File Edit View Build Tools Held 10 중 및 Ø | X =3 (2) ♥ (봄 ▶ ■ ♣ Topology 1 Properties X * Topology Application APP_1_Task.c* 9 \$include <L1_api.h> 10 \$include "L1_node_config.h" 11 \$include <StdioHostService/StdioHostClient.h> Configuration Source Semaphore_W_SP.ove readme.txt 12 13 void APP_1_Task (L1_TaskArguments Arguments) 14 { PutString(StdioHostServer, "This example demonstrates the Tasks synchronization mechani-Task1 and Task2 signal Sema1 and Sema2 by L1_SignalSemaphore_W\n\ Task1 and Task2 test Sema1 and Sema2 by L1_TestSemaphore_W\n\n Used waiting versions of SignalSemaphore and TestSemaphore functions(_W)\n\ Both tasks are placed on the same node, so its a single processor example\n\n\ Press Enter to start the example\n"); 15 16 17 18 19 20 21 22 GetChar(StdioHostServer); 23 24 while(1) 25 26 27 PutString(StdioHostServer, "Task 1 Signal Sema 1\n"); if (RC_OK != L1_SignalSemaphore_W (Sema1)) 28 29 30 PutString(StdioHostServer, "Not Ok\n"); . PutString(StdioHostServer, "Task 1 Test Sema 2\n"); 31 32 if (RC_OK != L1_TestSemaphore_W (Sema2)) 33 34 35 PutString(StdioHostServer, "Not Ok\n"); 3 3 36 • 37 } Files Nodes Entities Output Error List Ln 21 Col1 Define the behaviour of the tasks using C. 28/02/2010 Visit us at Booth 11-102 11



Performance	e of OpenComRTOS	Altreonic
 Code size figu Context Switch Interrupt Later 	res for different targets n Measurements ncy on an ARM Cortex M3	
28/02/2010	Visit us at Booth 11-102	13
Codesize Fig	gures	Altreonic

Service	MLX-16	MicroBlaze	Leon3	ARM	XMOS
L1 Hub shared	400	4756	4904	2192	4854
L1 Port	4	8	8	4	4
L1 Event	70	88	72	36	54
L1 Semaphore	54	92	96	40	64
L1 Resource	104	96	76	40	50
L1 FIFO	232	356	332	140	222
L1 PacketPool	NA	296	268	120	166
Total L1 Services	1048	5692	5756	2572	5414

Code size figures (in Bytes) obtained for our different ports, compiled with Optimisation Os

Semaphore Loop Performance



15

reon



To calculate the loop time the time for 1000 iterations gets taken, using the highest precision timer available in the system

Visit us at Booth 11-102

28/02/2010

Measured Loop Times

	Clock speed	Context size	Memory location	Loop time
MLX-16	6MHz	4 x16bit	internal	100.8µs
Xilinx Microblaze	100MHz	32 x 32bit	internal	33.6µs
Leon3	40MHz	32 x 32bit	external	136.1µs
ARM	50MHz	16 x 32bit	internal	52.7µs
XMOS	100MHz	14 x 32bit	internal	26.8µs

Interrupt Latency Measurement



17

ltreon

- Interrupt Latency is the time after an Interrupt Request (IRQ) occurred, until this message gets passed to a certain instance in the System.
- In OpenComRTOS we differentiate between two different Interrupt Latencies:

Visit us at Booth 11-102

- IRQ to ISR Latency
- IRQ to Task Latency

28/02/2010

Hardware Setup

- Device under Test:
 - CPU: 50MHz ARM Cortex-M3 (LM3s6965)
 - 64kB RAM
 - 256kB Flash
 - 50MHz timer / counter







System Application Diagram



28/02/2010

Visit us at Booth 11-102

Altreonic





IRQ to Task Latency	IRQ to ISR Latency	
Lin Log Reset Them	IRQ to ISR Latence	IRQ to Task Latency minimal: 13 usec maximal: 31 usec 98%: 29 usec samples: 1956
500		IRQ to ISR Latency minimal: 280 ns maximal: 2380 ns 98%: 2220 ns samples: 1955
200		
	2000 4000 5000 6000 700	Tns 0
I Connected		

Measured IRQ to Task Latency



28/02/2010

Visit us at Booth 11-102

Conclusions



23

- Advantages of the formal development:
 - Small code size (~10x smaller than Virtuoso from Eonic);
 - Higher Performance, due to less code to be executed;
 - Highly portable;
- Separation of topology and application resulted in a Virtual Single Processor (VSP) programming model.
- No failing malloc-operations, due to static allocation of memory during the build process.
- Support for systems consisting of different processor architectures.
- Supports for systems that use different communication technologies to represent Links.

28/02/2010

Visit us at Booth 11-102



